

Aditya Morey

Senior DFX/DFT Engineer - AI/HPC Hardware, Silicon Debug & Validation

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DFX/DFT engineer focused on hardware readiness, debug infrastructure, and validation methodology for AI and HPC accelerators. Depth across JTAG, scan, MBIST, and scan/RAM/array dump - IEEE 1149.1 / 1500 / 1687 - spanning pre-silicon verification through post-silicon bring-up, plus internal scan-debug GUI tooling used across teams.

EXPERIENCE

Senior DFX/DFT Engineer · NVIDIA

2024 - Present

- Own hardware readiness, debug infrastructure, and validation methodology for AI/HPC accelerators - JTAG, scan, MBIST, and scan/RAM/array dump across IEEE 1149.1 / 1500 / 1687.
- Drive pre-silicon verification and post-silicon bring-up, turning low-level silicon behavior into repeatable debug workflows.
- Build and maintain internal scan-debug GUI tooling used across multiple engineering teams; advance DFX security and Design-for-Debug (DFD) methodology.

Product Development Engineer · Intel

2021 - 2024

- Developed test methodologies, RTL, and test programs (C#/Perl) for repair, raster, and scan features on leading-edge process nodes, improving testing accuracy ~20%.
- Led pre-silicon validation for server products, boosting spec-validation efficiency ~15%.
- Improved scan-testing efficiency and reduced test time ~10%, driving yield enhancements and multi-million-dollar annual cost savings.
- Ran large-scale JMP data analysis, contributing to a ~20% yield increase and improved product reliability.

R&D Engineer · Zeda, Inc. (formerly PrinterPrezz)

2021

- Developed nanotextured coatings and selective-laser-melting 3D-printing processes for titanium and PEEK spinal implants; characterization and process optimization.

Research Assistant · Northeastern University

2020

- Designed and validated additive-manufactured titanium implants (selective laser melting), improving manufacturability and reducing production time.

EDUCATION

M.S., Mechanical Engineering (Materials Science)
B.Tech, Materials Science & Engineering

Northeastern University
IIT Kanpur

SELECTED CREDENTIALS

Granted US Patent US12172378B1 (additive manufacturing)
"The Cost of Usable Intelligence" (LCI)
"Designed to Be Debugged"

2024
SSRN working paper
Book - first research edition, 2026

SKILLS

DFT / DFX · Scan / ATPG / JTAG / MBIST · IEEE 1149.1 / 1500 / 1687 · Post-silicon validation · Silicon & secure debug · ASIC / SoC · AI accelerators · RTL · Perl · Tcl